UNITED STATES PATENT APPLICATION

For

GERMANIUM ON INSULATOR FABRICATION VIA EPITAXIAL GERMANIUM BONDING

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BACKGROUND

1. FIELD

[0001] This disclosure pertains to a method of fabricating a germanium-on-insulator (GOI) substrate and a method of bonding an epitaxial germanium layer to a semiconductor substrate to form a GOI substrate.

2. DISCUSSION OF RELATED ART

[0002] There is an increasing interest in using silicon-germanium (Si-Ge) alloy as a material for microelectronic and optoelectronic device applications. Germanium (Ge) is known to have high carrier mobility (e.g., high hole and electron mobility) and optical absorption as compared to silicon (Si). This is one reason why Ge is useful for devices that require enhanced performance and/or high quantum efficiency. Embodiments of devices that would benefit from the use of a Ge film include metal-oxide-semiconductor (MOS) transistors, optical detectors, and other optoelectronic devices, to name a few. There is also an increasing interest in bonding a germanium layer onto an insulator that is formed on a semiconductor substrate to form the GOI because the insulator layer in the semiconductor substrate helps reducing current leakage in the semiconductor device that is formed in the germanium layer.

[0003] There are generally two methods for forming a GOI substrate. In the first method, a crystalline Ge donor wafer is transferred (or bonded) onto a semiconductor wafer handle having an insulation layer. Ion exfoliation is then used to remove portions of the Ge donor wafer to leave a Ge layer bonded to the semiconductor wafer. Using a

crystalline Ge donor wafer to transfer Ge onto a wafer handle is costly. For instance, the crystalline Ge donor must be polished to the desired thickness which is time consuming and expensive. It is thus difficult and costly to remove surface non-uniformity after the ion exfoliation.

[0004] In the second method, an epitaxial Ge layer is formed on top of a semiconductor wafer handle having an insulation layer. Currently, an epitaxial Ge layer cannot be directly bonded to a wafer handle due to the high roughness inherent in the Ge layer. Direct wafer bonding requires smooth surfaces of about <0.5 nm to <1.5 nm RMS roughness. An epitaxial germanium (Ge) layer usually has a roughness of about >2 nm RM to >4nm RMS. Such roughness in an epitaxial Ge layer makes direct bonding of the Ge layer to an insulator on a semiconductor substrate (or wafer handle) difficult. In addition, to treat the surface of the epitaxial Ge so as to provide it with a smooth surface is difficult and expensive. For example, chemical mechanical polishing of an epitaxial Ge layer surface is time consuming.

[0005] There is thus a need for a new method of forming a GOI substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The disclosure is illustrated by way of embodiment and not by way of limitation in the figures of the accompanying drawings in which like references indicate similar elements. The invention may best be understood by referring to the following description and accompanying drawings that are used to illustrate embodiments of the invention. In the drawings:

[0007] **Figures 1A-1E** illustrate an exemplary GOI substrate at various stages of fabrication;

[0008] **Figures 2A-2F** illustrate another exemplary GOI substrate at various stages of fabrication;

[0009] **Figures 3A-3F** illustrate another exemplary GOI substrate at various stages of fabrication;

[0010] **Figure 4** illustrates an exemplary method of bonding an epitaxial Ge layer to a semiconductor substrate wafer in accordance to the embodiments of the present invention;

[0011] **Figure 5** illustrates another exemplary method of bonding an epitaxial Ge layer to a semiconductor substrate wafer in accordance to the embodiments of the present invention;

[0012] **Figure 6** illustrates yet another exemplary method of bonding an epitaxial Ge layer to a semiconductor substrate wafer in accordance to the embodiments of the present invention.

[0013] **Figure 7** illustrates a GOI substrate formed in accordance to some embodiments of the present invention;

[0014] **Figure 8** illustrates an exemplary semiconductor device (e.g., a transistor) that can be fabricated in a GOI substrate formed in accordance to some of the

embodiments of the present invention; and

[0015] **Figure 9** illustrates another exemplary semiconductor device (e.g., a detector) that can be fabricated in a GOI substrate formed in accordance to some of the embodiments of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0016] Exemplary embodiments are described with reference to specific configurations and techniques. Those of ordinary skill in the art will appreciate the various changes and modifications to be made while remaining within the scope of the appended claims. Additionally, well known elements, devices, components, circuits, process steps and the like are not set forth in detail.

[0017] The embodiments of the present invention direct to methods of forming a germanium-on-insulator (GOI) substrate. Throughout the disclosure, the term "bonded wafer pair" refers to a first semiconductor substrate having an epitaxial germanium layer formed thereon being bonded to a second semiconductor substrate. The first semiconductor substrate is bonded to a second semiconductor substrate through at least one dielectric layer. The term "semiconductor substrate" used in this disclosure includes a Si substrate, a Si-containing substrate, a Si substrate having an oxide layer (e.g., silicon dioxide), or a silicon-on-insulator (SOI) substrate. The silicon substrate may be monocrystalline, polycrystalline, or bulk silicon. The term "semiconductor substrate" may also include other material typically used to fabricate semiconductor devices such as gallium arsenide.

[0018] It is difficult to form a crystalline germanium layer on a dielectric layer. A dielectric layer is typically amorphous and as such, it is difficult for a crystalline

germanium layer to form thereon. Even if a germanium layer can be formed on a dielectric layer, it will be amorphous and lacking any crystalline structure. It is also difficult to bond an epitaxial germanium film onto a dielectric layer due to the inherent roughness of the epitaxial germanium film. The embodiments disclose methods of forming a GOI substrate that does not require bonding a germanium film onto a semiconductor substrate and does not required growing a germanium film on a dielectric layer. The embodiments disclose methods of forming a GOI substrate that includes forming a dielectric layer on an epitaxial germanium and then bonding that dielectric layer onto another surface to form the GOI substrate.

[0019] In one embodiment, an epitaxial Ge layer is formed on a first semiconductor substrate (e.g., Si substrate). The epitaxial Ge layer has a rough surface generally about 2nm or greater than 2nm RMS roughness. A first dielectric layer (e.g., silicon dioxide (SiO_2) or silicon nitride (Si_3N_4)) is formed over the epitaxial Ge layer, over the rough surface. The first dielectric layer conforms to the roughness pattern in the epitaxial Ge layer. The first dielectric layer is sufficiently thick to cover the roughness in the epitaxial Ge layer. A second semiconductor substrate (e.g., Si substrate) is provided. The first and the second semiconductor substrates are bonded together in a way that the first dielectric layer formed over the epitaxial Ge layer is bonded to a clean surface of the second semiconductor substrate. After the bonding, the first semiconductor substrate is removed and the structure remained is a GOI substrate. The GOI substrate includes the second semiconductor substrate, the dielectric layer, and the epitaxial Ge layer.

[0020] In an alternative embodiment, the second semiconductor substrate includes a second dielectric layer. When the first semiconductor substrate and the second semiconductor substrate are bonded together, the first dielectric layer and the second dielectric layer are directly bonded to each other. After the bonding, the first

semiconductor substrate is removed and the structure remained is a GOI substrate. The GOI substrate includes the second semiconductor substrate, the first and second dielectric layers, and the epitaxial Ge layer.

[0021] **Figures 1A-1E** illustrate various stages of forming a GOI substrate 100 in accordance to some embodiments of the present invention. In **Figure 1A**, a first semiconductor substrate 102 is provided. The first semiconductor substrate 102 can be any suitable material that an epitaxial Ge layer can be formed thereon and be removed from. The semiconductor substrate 102 is typically a Si wafer. It is to be appreciated that the Si wafer may be replaced by other suitable semiconductor substrate such as Ge and gallium arsenide.

[0022] In **Figure 1B**, an epitaxial Ge layer 104 is formed on top of the first semiconductor substrate 102. In one embodiment, the epitaxial Ge layer 104 has a surface with a roughness approximately greater than 2nm RMS. In another embodiment, the epitaxial Ge layer 104 has a surface with a roughness approximately greater than 4nm RMS. The epitaxial Ge layer 104 has a thickness 101 that may be less than 3000Å. In some embodiment, the epitaxial Ge layer 104 has a thickness 101 ranging from about 100-4000Å. The epitaxial Ge layer 104 can be formed using conventional methods such as chemical vapor deposition (CVD) or plasma enhanced CVP as is known in the art. In one embodiment, a germanium gas source (e.g., germane) is floated over the substrate 102, which creates a gas phase reaction with the surface of the first semiconductor substrate 102. The epitaxial Ge layer 104 is formed on the surface of the first semiconductor substrate 102 as a result of the gas phase reaction.

[0023] In **Figure 1C**, a dielectric layer 106 is formed over the epitaxial Ge layer 104. As shown in **Figure 1B**, the surface of the epitaxial Ge layer 104 is rough and thus difficult for a direct wafer bonding to the epitaxial Ge layer 104. Forming the dielectric

layer 106 over the epitaxial Ge layer 104 covers the rough surface on the epitaxial Ge layer 104 and allows bonding to the dielectric layer 106. In this way, the epitaxial Ge layer 104 can be bonded to another wafer through the dielectric layer 106.

[0024] The dielectric layer 106 is typically an oxide film such as silicon dioxide (SiO_2), silicon nitride (Si_3N_4), hafnium oxide (HfO_2), strontium tintanate ($SrTiO_3$), tantalum penta oxide (Ta_2O_5), titanium oxide (TiO_2), zirconium oxide (ZrO_2), aluminum oxide (Al_2O_3), and yttrium oxide (Y_2O_3), etc. The dielectric layer 106 can be a high-k dielectric layer or a low-k dielectric layer. It is more preferable to have a high-k dielectric layer 106 for a thinner and more efficient insulation layer. The dielectric layer 106 is compatible to a semiconductor substrate, which it will be bonded to, e.g., a silicon substrate. The dielectric layer 106 is formed by a conventional method such as CVD or plasma enhanced CVD.

[0025] In one embodiment, the dielectric layer 106 is sufficiently thick to cover the roughness on the surface of the epitaxial Ge layer 104. In one embodiment, the dielectric layer 106 has a thickness 103 greater than 3000Å. In another embodiment, the dielectric layer 106 has a thickness 103 greater than 6000Å. Portions of the dielectric layer 106 may be removed (e.g., by polishing or etching) to provide the dielectric layer 106 with a smaller thickness (e.g., a thickness 107 as shown in **Figure 1F** that is smaller than the thickness 103) if desired. In one embodiment, the thickness 103 is about 3000Å and the thickness 107 is about 500-2000 Å. In one embodiment, the dielectric layer 106 is polished using a conventional method such as chemical mechanical polishing (CMP) to remove some of the dielectric layer 106.

[0026] In **Figure 1D**, a second semiconductor substrate 110 is provided. The second semiconductor substrate 110 can be any suitable substrate typically used for

fabricating an electronic device therein. The second semiconductor substrate 110 can be a Si wafer.

[0027] In **Figure 1E**, the first semiconductor substrate 102 and the second semiconductor substrate 110 are bonded together. In particular, the first dielectric layer 106 is bonded to a surface of the second semiconductor substrate 110. After the bonding, the first dielectric layer 106 is buried between the second semiconductor substrate 110 and the epitaxial Ge layer 104.

[0028] A conventional bonding chamber can be used to bond the first semiconductor substrate 102 and the second semiconductor substrate 110 together. One embodiment of such conventional wafer-bonding chamber is the EVG 850 Series or the EVG 650 Series wafer bonders made by EV Group, Austria. An appropriate bonding condition for a wafer-bonding chamber is first obtained. The wafer-bonding chamber must be able to maintain the bonding temperature and bonding pressure. In one embodiment, the bonding temperature is obtained by heating up the wafer-bonding chamber to a desired bonding temperature, (e.g., a temperature ranging from 22°C to 600°C). In one embodiment, the bonding temperature is room temperature. In another embodiment, a chuck, which is used to hold the wafers, is heated up to the desired bonding temperature. The bonding pressure is obtained by evacuating the wafer-bonding chamber to a vacuum condition. The pressure of the wafer-bonding chamber can be obtained by using a conventional mechanical pump connected to the wafer-bonding chamber. The pressure of the wafer-bonding chamber is a pressure under which the mutual sticking of the Ge wafer to the Si wafer does not commence and that the Ge wafer and the Si wafer are held with respect to each other. In one embodiment, the pressure of the wafer-bonding chamber is below 1 Torr. In another embodiment, the pressure of the

wafer-bonding chamber is about 1 mili Torr. In another embodiment, the pressure is atmospheric pressure.

[0029] The wafer-bonding chamber provides a clean and dry environment for the bonding to occur. In addition, prior bonding, the surface of the first dielectric layer 106 and the surface of the surface of the second semiconductor substrate 110 that is to be bonded to the first dielectric layer 106 are cleaned so that they have clean, substantially particle free, and atomically smooth surfaces to facilitate a good bonding. The present of small particles (e.g., particles having size larger than about 0.1-0.2 μm) would interrupt the bonding of the wafers and lead to void and decreasing bonding strength.

[0030] In one embodiment, a moisture containing carrier gas such as nitrogen, xenon and helium is introduced into the wafer-bonding chamber at a flow rate of about 10 ml-100 ml per minute to facilitate the bonding.

[0031] The bonding may occur with either the second semiconductor substrate 110 or the first semiconductor substrate 102 being on the bottom or being on top. In one embodiment, the second semiconductor substrate 110 is placed on the chuck in the bonding chamber and the first semiconductor substrate 102 is place on the top of the second semiconductor substrate 110 with the first dielectric layer 104 facing the second semiconductor substrate 110 for bonding.

[0032] A local force is applied either to the to the first semiconductor substrate 102 or the second semiconductor substrate 110 to initiate the bonding. In one embodiment, the local force is a force applied to one point either on the first semiconductor substrate 102 or the second semiconductor substrate 110. In another embodiment, the local force is applied to a region near an edge of either the first semiconductor substrate 102 or the second semiconductor substrate 110 using a Teflon pin conveying a force ranging from 3 Newton to 4000 Newton pressing down on that

region. In a preferred embodiment, the local force is about 2000 Newton. Once the bonding is initiated, the bonding is propagated to completely bond the first dielectric layer 104 to the second semiconductor substrate 110. In one embodiment, the bonding is allowed to continue for an amount of time (e.g., 30 seconds or more) sufficient to completely bond the first dielectric layer 104 to the second semiconductor substrate 110 to form a bonded wafer pair.

[0033] After the bonding, the first semiconductor substrate 102 is removed using methods such as etching, grinding, and/or ion exfoliation. Ion exfoliation generally refers to a process that uses ion implantation to implant ions into a substrate such as the first semiconductor substrate 102, to a predetermined depth. The ions implanted form a cleaving plane at the predetermined depth within the substrate. The substrate can then be cleaved at the cleaving plane and be removed. After the first semiconductor substrate 102 is removed, the remaining structure forms the GOI substrate 100.

[0034] In one embodiment, prior to the removal of the first semiconductor substrate 102, the bonded wafer pair is annealed to strengthen the bonding interface and the bonding of the bonded wafer pair. The annealing process removes and diffuses any moisture trapped at the interface of the first dielectric layer 106 and the second semiconductor substrate 110. In one embodiment, the annealing process takes place in the same wafer-bonding chamber that is used for the bonding. The annealing process occurs at a temperature that is sufficient to strengthen the bonded wafer pair without causing damages to the bonded wafer pair. There are several ways for annealing the bonded wafer pair. In one embodiment, the bonded wafer pair is annealed at a temperature greater that 100°C. The annealing temperature can be as high as 600°C or as high as 75% of the melting temperature of the wafers. In another embodiment, the bonded wafer pair is annealed in the presence of a carrier gas such as nitrogen and at a

temperature of about 150°C. In one embodiment, the annealing temperature (e.g., 100-150°C) is obtained with the temperature being ramped up to the annealing temperature at a rate of 1°C/minute while the bonded wafer pair resides in the chamber. After the annealing temperature is obtained, the bonded wafer pair is held in the chamber for a predetermined amount of time sufficient to anneal the bonded wafer pair, e.g., 1-20 hours. It is more advantageous to anneal the bonded wafer pair at a lower temperature and longer duration to prevent damages to the bonded wafer pair. The bonded wafer pair is then allowed to cool down with the temperature ramping down at a rate of approximately 1°C/minute to 2°C/minute. It is to be appreciated that the bonded wafer pair may be annealed using conventional annealing methods and that the annealing conditions recited above is only an exemplary condition and not a limitation.

[0035] In the embodiments where the bonded wafer pair is annealed, the first semiconductor substrate 102 is removed after the annealing to yield the GOI substrate 100. In the embodiments shown in **Figures 1A-1E**, the first semiconductor substrate 102 can be removed by grinding back (e.g., using CMP) to expose the epitaxial Ge layer 104. Alternatively, the first semiconductor substrate 102 can be removed by an etching process to expose the epitaxial Ge layer 104. Alternatively yet, the first semiconductor substrate 102 can be removed by a combination of a grind back and an etching processes. After the first semiconductor substrate 102 is removed, the GOI is formed having the epitaxial Ge layer 104 and the dielectric layer 106 bonded to the second semiconductor substrate 110.

[0036] In one embodiment, the first semiconductor substrate 102 is partially removed by a grind back process. The first semiconductor substrate 102 can then be polished using a CMP process to remove the majority of the first semiconductor substrate 102 from the bonded wafer pair. The first semiconductor substrate 102 can also be

etched away using a chemistry that is selective to remove the substrate 102 to complete the removal process of the substrate 102.

[0037] **Figures 2A-2F** illustrate various stages of forming a GOI substrate 200 in accordance to some embodiments of the present invention. The GOI substrate 200 is similar to the GOI substrate 100 except that the second semiconductor substrate includes an additional dielectric layer.

[0038] In **Figure 2A**, a first semiconductor substrate 202 is provided. The first semiconductor substrate 202 can be any suitable material that an epitaxial Ge layer can be formed thereon and be removed from. The semiconductor substrate 202 is typically a Si wafer.

[0039] In **Figure 2B**, an epitaxial Ge layer 204 is formed on top of the first semiconductor substrate 202. In one embodiment, the epitaxial Ge layer 204 has a surface with a roughness approximately greater than 2nm RMS. In another embodiment, the epitaxial Ge layer 204 has a surface with a roughness approximately greater than 4nm RMS. The epitaxial Ge layer 204 has a thickness 201 that may be less than 3000Å. In some embodiment, the epitaxial Ge layer 204 has a thickness 201 ranging from about 100-4000Å. The epitaxial Ge layer 204 can be formed using conventional methods such as chemical vapor deposition (CVD) or plasma enhanced CVP as is known in the art.

[0040] In **Figure 2C**, a first dielectric layer 206 is formed over the epitaxial Ge layer 204. As shown in **Figure 2B**, the surface of the epitaxial Ge layer 204 is rough and thus difficult for a direct wafer bonding to the epitaxial Ge layer 204. Forming the first dielectric layer 206 over the epitaxial Ge layer 204 covers the rough surface on the epitaxial Ge layer 204 and allows bonding to the first dielectric layer 206. In this way, the epitaxial Ge layer 204 can be bonded to another wafer through the first dielectric layer 206. The first dielectric layer 206 is similar to the dielectric layer 106 previously

described and can be an oxide film such as SiO_2, Si_3N_4, HfO_2, $SrTiO_3$, Ta_2O_5, TiO_2, ZrO_2, Al_2O_3, and Y_2O_3, etc. The first dielectric layer 206 is formed by a conventional method such as CVD or plasma enhanced CVD.

[0041] In one embodiment, the first dielectric layer 206 is sufficiently thick to cover the roughness on the surface of the epitaxial Ge layer 204. In one embodiment, the first dielectric layer 206 has a thickness 203 greater than 3000Å. In another embodiment, the first dielectric layer 206 has a thickness 203 greater than 6000Å. Portions of the first dielectric layer 206 may be removed (e.g., by polishing or etching) to provide the first dielectric layer 206 with a smaller thickness (e.g., a thickness 207 as shown in **Figure 2F** that is smaller than the thickness 203) if desired. In one embodiment, the thickness 203 is about 3000Å and the thickness 207 is about 500-2000Å. In one embodiment, the first dielectric layer 206 is polished using a conventional method such as chemical mechanical polishing (CMP) to remove some of the first dielectric layer 206.

[0042] In **Figure 2D**, a second semiconductor substrate 210 is provided. The second semiconductor substrate 210 can be any suitable substrate typically used for fabricating an electronic device therein. The second semiconductor substrate 210 can be a Si wafer.

[0043] In **Figure 2E**, a second dielectric layer 212 is formed on top of the second semiconductor substrate 210. The second dielectric layer 212 is similar to the first dielectric layer 206 and can be formed of similar material and using similar methods as those used for the first dielectric layer 206. The second dielectric layer 212 has a predetermined thickness 205. The second dielectric layer 212 and the first dielectric layer 206 should have a combined thickness 209 that is sufficient to insulate the device that will be formed on the GOI substrate 200. In one embodiment, the combined thickness 209 is between 500-3500Å.

[0044] In **Figure 2F**, the first semiconductor substrate 202 and the second semiconductor substrate 210 are bonded together. In particular, the first dielectric layer 206 is bonded to the second dielectric layer 212. After the first bonding, the first dielectric layer 206 and the second dielectric layer 212 are buried between the first semiconductor substrate 202 and the epitaxial Ge layer 204. The bonding condition and chamber are similar to the one used for form the GOI substrate 100 previously described. The first semiconductor substrate 202, the epitaxial Ge layer 204, the first dielectric layer 206, the second dielectric layer 212, and the second semiconductor substrate 210 form a bonded wafer pair after the bonding.

[0045] After the bonding, the first semiconductor substrate 202 is removed and the remaining structure forms the GOI substrate 200. In one embodiment, prior to the removal of the first semiconductor substrate 202, the bonded wafer pair is annealed using conventional methods or methods previously described to strengthen the bonding interface. In one embodiment, the first semiconductor substrate 202 is removed by grinding back (e.g., using CMP) to expose the epitaxial Ge layer 204. Alternatively, the first semiconductor substrate 202 is removed by an etching process to expose the epitaxial Ge layer 204. Alternatively yet, the first semiconductor substrate 202 can be removed by a combination of a grind back and an etching processes. The first semiconductor substrate 202 can also be removed similarly to the removal of the first semiconductor substrate 102 previously described. After the first semiconductor substrate 202 is removed, the GOI 200 is formed having the epitaxial Ge layer 204, the first and second dielectric layers 206 and 212 bonded to the second semiconductor substrate 210.

[0046] **Figures 3A-3F** illustrate various stages of forming a GOI substrate 300 in accordance to some embodiments of the present invention. The GOI substrate 300 is

similar to the GOI substrate 100 and 200 except that the first semiconductor substrate includes a cleaving plane 311 for facilitate the removal of the first semiconductor substrate after the bonding. In addition, the second semiconductor substrate may optionally but need not include a second dielectric layer 312.

[0047] In **Figure 3A**, a first semiconductor substrate 302 is provided. The first semiconductor substrate 302 can be any suitable material that an epitaxial Ge layer can be formed thereon and be removed from. The semiconductor substrate 302 is typically a Si wafer.

[0048] In **Figure 3B**, an epitaxial Ge layer 304 is formed on top of the first semiconductor substrate 302. In one embodiment, the epitaxial Ge layer 304 has a surface with a roughness approximately greater than 2nm RMS. In another embodiment, the epitaxial Ge layer 304 has a surface with a roughness approximately greater than 4nm RMS. The epitaxial Ge layer 304 has a thickness 301 that may be less than 3000Å. In some embodiment, the epitaxial Ge layer 304 has a thickness 301 ranging from about 100-4000Å. The epitaxial Ge layer 304 can be formed using conventional methods such as chemical vapor deposition (CVD) or plasma enhanced CVP as is known in the art.

[0049] In **Figure 3C**, a first dielectric layer 306 is formed over the epitaxial Ge layer 304. As shown in **Figure 3B**, the surface of the epitaxial Ge layer 304 is rough and thus difficult for a direct wafer bonding to the epitaxial Ge layer 304. Forming the first dielectric layer 306 over the epitaxial Ge layer 304 covers the rough surface on the epitaxial Ge layer 304 and allows bonding to the first dielectric layer 306. In this way, the epitaxial Ge layer 304 can be bonded to another wafer through the first dielectric layer 306. The first dielectric layer 306 is similar to the dielectric layer 106 previously described and can be an oxide film such as SiO_3, Si_3N_4, HfO_3, $SrTiO_3$, Ta_3O_5, TiO_3,

ZrO_3, Al_3O_3, and Y_3O_3, etc. The first dielectric layer 306 is formed by a conventional method such as CVD or plasma enhanced CVD.

[0050] In one embodiment, the first dielectric layer 306 is sufficiently thick to cover the roughness on the surface of the epitaxial Ge layer 304. In one embodiment, the first dielectric layer 306 has a thickness 303 greater than 3000Å. In another embodiment, the first dielectric layer 306 has a thickness 303 greater than 6000Å.

[0051] In **Figure 3C**, ion implantation 320 is used to bombard ions (e.g., hydrogen ion) into the first semiconductor substrate 302. The ion implantation 320 creates a cleaving plane 311 that later facilitates the removal of the first semiconductor substrate 302 after bonding. The cleaving plane 311 can be created at a location that is convenient for the removal of the first semiconductor substrate 302 after the bonding. In one embodiment, the ion implantation 320 bombards ions into the first semiconductor substrate 302 at a location near the interface 313 between the epitaxial Ge layer 204 and the first semiconductor substrate 302. The ion implantation 320 may be deeper into the first semiconductor substrate 302 if desired. In one embodiment, a conventional ion implantation process is used to implant energetic particles or ions (e.g., hydrogen particles, H_2^+ or H^+) through the top surface of the first dielectric layer 306 to a predetermined depth in the first semiconductor substrate 302. The cleaving plane is parallel or substantially parallel to the surface of the first dielectric layer 306. In one embodiment, the ions are implanted to a dosage of about $5X10^{16}$ to $5X10^{18}$, or $1X10^{17}$. A smoothing process can be used after the first semiconductor substrate 302 is cleaved off to smooth out the surface for the epitaxial Ge layer 304.

[0052] In one embodiment, portions of the first dielectric layer 306 are removed (e.g., by polishing or etching) to provide the first dielectric layer 306 with a smooth, substantially particle free, and clean surface (to repair any damages caused by the ion

implantation). A smooth surface will facilitate the bonding of the first dielectric layer 306 to another surface. In addition, the first dielectric layer 306 may be thinned to a desired thickness in the removal process. For some embodiments, the first dielectric layer 306 may be thinned from the thickness 303 to a thickness 307 shown in **Figure 3F** that is smaller than the thickness 303. In one embodiment, the thickness 303 is about 3000Å and the thickness 307 is about 500-2000Å. In one embodiment, the first dielectric layer 306 is polished using a conventional method such as chemical mechanical polishing (CMP) to remove some of the first dielectric layer 306.

[0053] In **Figure 3D**, a second semiconductor substrate 310 is provided. The second semiconductor substrate 310 can be any suitable substrate typically used for fabricating an electronic device therein. The second semiconductor substrate 310 can be a Si wafer.

[0054] In **Figure 3E**, a second dielectric layer 312 is formed on top of the second semiconductor substrate 310. The second dielectric layer 312 is similar to the first dielectric layer 306 and can be formed of similar material and using similar methods as those used for the first dielectric layer 306. The second dielectric layer 312 has a predetermined thickness 305. The second dielectric layer 312 and the first dielectric layer 306 should have a combined thickness 309 that is sufficient to insulate the device that will be formed on the GOI substrate 300. In one embodiment, the combined thickness 309 is between 500-3500Å.

[0055] In **Figure 3F**, the first semiconductor substrate 302 and the second semiconductor substrate 310 are bonded together. In particular, the first dielectric layer 306 is bonded to the second dielectric layer 312. After the bonding, the first dielectric layer 306 and the second dielectric layer 312 are buried between the first semiconductor substrate 302 and the epitaxial Ge layer 304. The bonding condition and chamber are

similar to the one used for form the GOI substrate 100 previously described. The first semiconductor substrate 302, the epitaxial Ge layer 304, the first dielectric layer 304, the second dielectric layer 312, and the second semiconductor substrate 310 form a bonded wafer pair after the bonding. After the bonding, the first semiconductor substrate 302 is removed and the remaining structure is the GOI substrate 300.

[0056] In one embodiment, prior to the removal of the first semiconductor substrate 302, the bonded wafer pair is annealed using conventional methods or methods previously described to strengthen the bonding interface. In one embodiment, the first semiconductor substrate 302 is removed a nitrogen jet to initiate the cleaving of the first semiconductor substrate 302 at the cleaving plane 311. Alternatively, the first semiconductor substrate 302 is removed by an annealing process to thermally cleave the first semiconductor substrate 302 at the cleaving plane 311. The annealing process used to thermally cleave the first semiconductor substrate 302 can be similar to the annealing process used to strengthen the bonding of the bonded wafer pair. The annealing process used to thermally cleave the first semiconductor substrate 302 typically occurs at a temperature that is sufficient to initiate the cleaving of the first semiconductor substrate 302. The cleaving temperature ranges from 100°C to 600°C. In one embodiment, the cleaving temperature is approximately 150°C for ion implantation that creates a cleaving plane within the epitaxial Ge layer 304. In another embodiment, the cleaving temperature is approximately 450°C for ion implantation that creates a cleaving plane within the first semiconductor substrate 302.

[0057] The removal of the first semiconductor substrate 302 exposes the epitaxial Ge layer 304. After the first semiconductor substrate 302 is removed, the GOI 300 is formed having the epitaxial Ge layer 304, the first and second dielectric layers 306 and 312 bonded to the second semiconductor substrate 310.

[0058] In one embodiment, after cleaving, the epitaxial Ge layer 304 may have a rough surface on the side where the first semiconductor substrate 302 was removed. The epitaxial Ge layer 304 may be polished (and if needed, further thinned) using a chemical mechanical polishing (CMP), a wet chemical treatment, or wet/dry etching method well known in the art. In one embodiment, a conventional CMP tool is used to polish and/or to repair any surface damage and/or roughness in the epitaxial Ge layer 304.

[0059] **Figure 4** illustrates an exemplary embodiment of a method 400 of forming a GOI substrate (e.g., the GOI substrate 100). At operation 402, an epitaxial Ge layer is formed on top of a first semiconductor substrate, which may be a Si wafer. At operation 404, a first dielectric film (e.g., an oxide or a nitride film) is formed on top of the epitaxial Ge layer. At operation 606, a second semiconductor substrate is provided. The second semiconductor substrate may have a second dielectric film formed on top of the second semiconductor substrate. At operation 608, the first semiconductor substrate is bonded to the second semiconductor substrate in such a way that the first dielectric film is bonded to the second semiconductor substrate or alternatively, the first dielectric film is bonded to the second dielectric film. At operation 610, the first semiconductor substrate is removed to expose the epitaxial Ge layer, e.g., by using a grind back and/or an etching process.

[0060] **Figure 5** illustrates another exemplary method 500 of forming a GOI substrate (e.g., the GOI substrate 300). At operation 502, an epitaxial Ge layer is formed on top of a first semiconductor substrate, which may be a Si wafer. At operation 504, a first dielectric film (e.g., an oxide or a nitride film) is formed on top of the epitaxial Ge layer. At operation 506, ion implantation is used to implant particles into the first semiconductor substrate. In one embodiment, the ions are implanted into the first

semiconductor substrate using hydrogen implantation. The ion implantation creates a cleaving plane within the first semiconductor substrate.

[0061] At operation 508, a second semiconductor substrate is provided. The second semiconductor substrate may have a second dielectric film formed on top of the second semiconductor substrate. At operation 510, the first semiconductor substrate is bonded to the second semiconductor substrate in such a way that the first dielectric film is bonded to the second semiconductor substrate or alternatively, the first dielectric film is bonded to the second dielectric film. At operation 512, the first semiconductor substrate is removed to expose the epitaxial Ge layer, e.g., by using a thermal cleaving process or jetting process.

[0062] **Figure 6** illustrates another exemplary method 600 of forming a GOI substrate (e.g., the GOI substrate 300). At operation 602, an epitaxial Ge layer is formed on top of a first semiconductor substrate, which may be a Si wafer. At operation 604, a first dielectric film (e.g., an oxide or a nitride film) is formed on top of the epitaxial Ge layer. At operation 606, ion implantation is used to implant particles into the first semiconductor substrate. In one embodiment, the ions are implanted into the first semiconductor substrate using hydrogen implantation. The ion implantation creates a cleaving plane within the first semiconductor substrate. In addition, the first dielectric layer is polished (e.g., using CMP or etching) to provide a smooth and/or flat surface for bonding. The polishing process occurs after the ion implantation to repair any damages to the surface of the first dielectric layer.

[0063] At operation 608, a second semiconductor substrate is provided. The second semiconductor substrate may have a second dielectric film formed on top of the second semiconductor substrate. At operation 610, the first semiconductor substrate is bonded to the second semiconductor substrate in such a way that the first dielectric film

is bonded to the second semiconductor substrate or alternatively, the first dielectric film is bonded to the second dielectric film. At operation 612, the first semiconductor substrate is removed to expose the epitaxial Ge layer, e.g., by using a thermal cleaving process or jetting process.

[0064] **Figure 7** illustrates an exemplary GOI substrate 700 formed in accordance to some of the embodiments of the present invention. The GOI substrate 700 can be the GOI substrate 100, 200, 300, or 400 previously described. The GOI substrate 700 includes a semiconductor substrate 710, which is bonded to a dielectric layer 712 and a dielectric 706. The dielectric layer 706 is formed over an epitaxial Ge layer 704 as previously described. In certain embodiments, the dielectric layer 712 is eliminated and only the dielectric layer 706 is present and bonded to the semiconductor substrate 710 as previously described.

[0065] **Figure 8** illustrates an exemplary semiconductor device 701 fabricated in the GOI substrate 700. In one embodiment, the semiconductor device 701 is a transistor. The semiconductor device 701 includes the GOI substrate 700, isolation trenches 720, source drain regions 748, a gate dielectric 742, a gate electrode 744, spacers 746, and optionally, source/drain contacts 700.

[0066] In one embodiment, the epitaxial Ge layer 704 of the GOI substrate 700 may be moderately doped (e.g., $1x10^{16}$ per cm^3 to $1x10^{15}$ per cm^3). The doping concentration is chosen to properly target the transistor threshold voltage. Isolation trenches 720 may be formed into the Ge layer 704 using conventional methods (e.g., etching). The gate dielectric 742, gate electrode 744, and spacers 746 can be formed on the top surface of the Ge layer 704 using conventional methods (e.g., film deposition and patterning). In one embodiment, the gate dielectric 742 is made out of a high-k dielectric material. The gate electrode 744 can be made out of a metal containing material, such as

titanium nitride or tungsten, for a metal gate. The gate electrode 744 can also be doped polysilicon. The spacers 746, typically comprise of a combination of SiO_2 and Si_3N_4. The source and drain regions 748 are formed in the Ge layer 704 using conventional methods. The source and drain regions 748 may be heavily doped with a dopant concentration of $1x10^{20}$ per cm^3.

[0067] Source/drain contacts 740 can be made of nickel-germanium (NiGe) and formed on the Ge layer 704 over the regions that are not covered by the gate dielectric 742 and the spacers 746. In one embodiment, the NiGe is formed by a low-temperature annealing method using an annealing temperature of about 400°C to 600°C. Depositing a metal (e.g., nickel) that reacts with the material in the transistor body can substantially lower the resistivity of the source and drain contacts. Conventional contacts can also be formed instead to establish contacts to the source/drain regions 748.

[0068] Those skilled in the art will recognize that the features mentioned in **Figure 5** and other features may be used or may be left out, depending upon the particular function of the device 701. For some embodiments, after the formation of the NiGe, the device 701 is subjected to convention process of forming interlayer dielectric deposition, contact patterning, metalization, etc.

[0069] **Figure 9** illustrates another exemplary semiconductor device 702 that can be fabricated in the GOI substrate 700. The exemplary semiconductor device 702 is an integrated detector that may provide electrical output driven by an optical input to integrated circuits in a substrate. The device 702 includes the GOI substrate 700 having the epitaxial Ge layer 704. Isolation trenches 720 are formed into the epitaxial Ge layer 704 using conventional methods. The device 702 further includes a waveguide 752 formed on top of the epitaxial Ge layer 704 using conventional methods. The waveguide 752 is further encapsulated by a dielectric layer 750. It is common for the integrated

structure to have the waveguide 752 be made out of a relatively high-refractive index material (e.g., Si_3N_4 which has a refractive index n=2.05). The waveguide 752 is typically encapsulated in a material with lower refractive index (e.g., SiO_2 which has a refractive index n=1.46). When light is introduced in the waveguide 752 having the high refractive index material, the light will be confined there. The waveguide 752 then "guides" the light from the source (typically an external laser) to the detector (in this case, the Ge layer 704).

[0070] Detector electrodes 754 are formed in vias created in the dielectric layer 750. In order for the Ge layer 704 to function as a detector, a bias must be applied across it. Any light shining on the detector then generates electron-hole pairs. These pairs are swept by the bias field, causing current to flow through the Ge layer 704. There is an electrical response to a light impulse. The detector electrodes 754 are needed to provide the required bias. In one embodiment, a conductive material, such as metal, is deposited and then patterned using conventional methods. In this embodiment, the detector electrodes 754 are deposited by a damascene process, well practiced in the field.

[0071] While the invention has been described in terms of several embodiments, those of ordinary skill in the art will recognize that the invention is not limited to the embodiments described. The method and apparatus of the invention, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of limiting.

[0072] Having disclosed exemplary embodiments, modifications and variations may be made to the disclosed embodiments while remaining within the spirit and scope of the invention as defined by the appended claims.